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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Tai A. Ly et al.

Art Unit: **2825**

Application No. **09/590,584**

Examiner: **A. Thompson**

Filed: **Jun. 8, 2000**

Confirmation No. **1223**

For: **Methods For Automatically
Pipelining Loops**

Attorney Docket: **SNPS.0024REI**
(Prior Docket No. 4000/10)

Appeal Brief

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir or Madam:

In response to the final Office Action mailed Aug. 16, 2005, and subsequent to the Notice of Appeal received by the USPTO on Feb. 21, 2006, applicants submit the present Appeal Brief on Jul. 20, 2006.

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(i) Real party in interest

The real party in interest is the assignee of the present application, Synopsys, Inc., 700 East Middlefield Rd, Mountain View, CA 94043.

(ii) Related appeals and interferences

There are no related appeals or interferences.

(iii) Status of claims

Claims 1-40 are pending. Claims 1-34 have been allowed. Claims 35-40 are rejected and are being appealed.

(iv) Status of amendments

In response to a final Office Action with a date mailed of August 16, 2005, that rejects claims 35-40, applicants submitted a Notice of Appeal that was received by the Patent Office on Feb. 21, 2006.

Subsequent to the Notice of Appeal, but prior to the submission of the present Appeal Brief, an Amendment was filed July 7, 2006. The July 7 Amendment is submitted to correct a minor typographical error to permit the rejected claims to be presented in better form for consideration on appeal. Specifically, the Amendment makes claim 35 dependent on claim 1 rather than claim 2. Claims Appendix (viii) is written including the change to claim 35 that is called for by the July 7 Amendment.

The July 7 Amendment is currently in the Image File Wrapper. On July 12 the July 7 Amendment was forwarded to the Examiner for her consideration. On July 17 an Advisory Action (PTOL-303) was created. As of the date of submission of this Appeal Brief, however, the contents of the July 17 Advisory Action is not available online through the USPTO PAIR interface.

(v) Summary of claimed subject matter

Appealed claims 35-37 depend on, respectively, independent claims 1, 18 and 21. Appealed claims 38-40 are independent claims. Therefore, a concise explanation of the subject matter of the following independent claims shall be provided: 1, 18, 21,

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38-40.

Claims 18 and 21 are, respectively, system and computer program product versions of method claim 1. Therefore, a concise explanation shall be provided for claim 1 that shall suffice to provide a concise explanation for claims 18 and 21.

Claims 39 and 40 are, respectively, system and computer program product versions of claim 38. Therefore, a single concise explanation shall be provided for claim 38 that shall suffice to provide a concise explanation for claims 39 and 40.

In accordance with 37 CFR 41.37(c)(1)(v), the concise explanations shall be presented by way of reference to the example embodiment of the specification and drawings.

Page 9, lines 2-4, of the specification summarize the invention as follows:

The present invention is a method and apparatus for synthesizing a circuit which implements a pipelined loop from a Hardware Description Language (HDL) description.

The specification, from page 4, line 17 to page 5, line 12, describes a pipelined loop as follows:

In some loops, data required by an operation in the next loop iteration is available prior to completion of the current loop. Under these conditions, the designer can *pipeline* the loop--parallelizing execution of iterations to increase throughput beyond critical path limitations of the loop body. This process of loop pipelining schedules consecutive loop iterations to partially overlap in time; a new loop iteration is initiated before the current iteration has finished.

Figure 2 shows an example of loop pipelining where the data required by operation A in iteration two is available after operation C in the first loop iteration.

The two timing-related aspects of a loop that affect throughput are:

Initiation interval: The number of clock cycles between the start of two consecutive loop iterations.

Latency: The number of clock cycles required to execute all operations in a single loop iteration.

For sequential loops that are not pipelined, the initiation interval and latency of a loop are the same. For a pipelined loop, the initiation interval is smaller than the latency.

The primary reason for using loop pipelining is to

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increase the throughput of the design; the trade-off is that the design area usually increases.

Many designs have separate specifications on throughput and input-to-output delay. The throughput specification constrains the initiation interval. The input-to-output delay specification constrains the loop latency. Loop pipelining enables a flexible relationship between the initiation interval and latency of a loop.

An example of a candidate for loop pipelining is a design that processes a data stream. This type of design often has tight throughput requirements based on the rate of the data streams and loose input-to-output delay constraints.

An overall process, in which the steps of claims 1 and 38 can be embodied, is presented through Figure 6. Figure 6 is discussed, in the specification, at such locations as page 14, lines 21-24. Further details, of Figure 6, are presented in Figures 7-9 which are discussed, in the specification, at such locations as page 14, line 25 to page 15, line 11.

Regarding claim 38, an example (of the claimed) "text description of a circuit" is shown in Figure 11. Figure 11 depicts (the claimed) "N clock statements," where $N=2$, where each clock statement is the Verilog statement "@(posedge clock)." An example (of the claimed) "digital circuit representation," for Figure 11, is shown in Figure 14. The digital circuit representation of Figure 14 includes a pipeline and (the claimed) "initiation interval of said pipeline equal to N" (i.e., the initiation interval is two). Production of Figure 14 from Figure 11 is described in the specification at the following location: page 19, line 18 to page 20, line 23.

Regarding claim 1, an example (of the claimed) "text description of a circuit" with a (claimed) "delayed signal assignment" is shown in Figures 19(a) and 19(b). The processing, of this example input, is discussed in section 5 of the specification ("Circuit Synthesis using Delayed Signal Assignment Information") that starts at page 22, line 16 and ends at page 28, line 10. The (claimed) "delay value" is depicted in Figure 19(a) as "#24" and in Figure 19(b) as "after 24 ns." An example (of the claimed) "digital circuit representation," for Figures 19(a) and 19(b), is shown in Figure 14. Figure 14 is discussed in the specification at the following location: page 27, line 8. Production of a (claimed) "pipeline," with a (claimed) "latency ... equal to said delay value," is shown in Figures 25 and 26 that are described in the specification at the following location: page 27, line 17 to page 28, line 4.

(vi) Grounds of rejection to be reviewed on appeal

Each of the following grounds of rejection to be reviewed upon appeal is addressed in a correspondingly numbered subsection of the "Argument" section (vii) below:

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1. Whether Appendices A and B are part of the original disclosure as filed and available as claimable subject matter.
2. Whether applicants are able to put Appendices A and B in formal form or whether such formalization constitutes new matter.
3. Whether incorporation by reference of Appendices A and B is improper because, at the time of filing, Appendices A and B were unpublished.
4. The extent of incorporation by reference of Appendices A and B.
5. Whether claims 35-40 are to be rejected for being based upon new matter from Appendix B.
6. Whether claims 35-40 are not enabled due to their being based upon new matter from Appendix B.
7. Whether applicants presentation to the Examiner, of the applicants discussions with the USPTO Office of Patent and Legal Administration, was improper.

(vii) Argument

Note re Abbreviations

In the following numbered sections of the Argument, the following abbreviations are used to refer to documents of the file history:

OA2: Refers to the 2nd Office Action on the merits in the present reissue application that has a date mailed of Feb. 20, 2004.

RT OA2: Refers to applicants response to OA2 that has a certificate of mailing date of Mar. 22, 2004.

OA3: Refers to the 3rd Office Action on the merits in the present reissue application that has a date mailed of Jan. 14, 2005.

RT OA3: Refers to applicants response to OA3 that has a certificate of transmission date of July 14, 2005.

OA4: Refers to the 4th Office Action on the merits in the present reissue application that has a date mailed of Aug. 16, 2005.

1. Original Disclosure

The claims involved in this appeal, were rejected in paragraph 5 of OA3 as based on new matter. The Examiner states:

The added material which is not supported by the prior patent is as follows:

Applicants' specification, without the improperly incorporated appendices does not include support for the term "clock statement".

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In addition, the Examiner states:

The added material which is not supported by the original disclosure is as follows: The Appendices and the new drawings.

OA3, paragraph 4.

In their response to OA3, applicants state the following:

Applicants respectfully direct the Examiner's attention to the fact that incorporation by reference is not the only basis upon which the subject matter of Appendices A and B is part of the present application.

In addition to incorporating Appendices A and B by reference, the formal specification makes plain that Appendices A and B are also part of the specification itself.

The formal specification uses the word "appendix" to refer to Appendices A and B. The word "appendix" means an addition of subject matter to a document.

In referring to Appendices A and B, after providing a publication citation corresponding to each appendix, the formal specification states that each appendix "is included."

In addition to the language of the formal specification, Appendices A and B were, in fact, included with the formal specification as originally filed on May 12, 1995. Evidence of this includes the stamped postcard receipt listing these appendices along with the formal specification.

RT OA3, page 12 of 14.

In the subsequent Office Action the Examiner appears to admit that Appendices A and B are part of the original filing. The Examiner states:

The patent Appendices A and B, although part of the original filing, were not part of the printed patent because they were contained on pages located after the claims. In the instant reissue application, Applicants have amended the specification and added most of the text of the Appendices before the claims, ostensibly to enable the printing of the Appendices upon issuance.

OA4, paragraph 5 (emphasis added). However, later on in OA4 claims 35-40 are still rejected under 35 USC § 251 as based upon new matter from Appendix B. Specifically, the Examiner states:

Applicants' formal specification as originally filed does not include support for the term "clock statement".

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Applicants' Appendices A and B may not be referenced in the specification as being "incorporated by reference".

OA4, paragraph 15.

Applicants respectfully request a unambiguous statement that Appendices A and B are part of the original filing and are therefore available as claimable subject matter.

2. Formalizing Appendices A and B

As discussed above in section 1 ("Original Disclosure"), in paragraph 5 of OA4 the Examiner appears to admit that Appendices A and B are part of the original filing.

Nevertheless, in paragraph 7 of OA4, the Examiner rejects applicants formalization of Appendices A and B, and seems to only permit a movement of the appendices, as-is, to a location prior to the claims. Specifically, in paragraph 7 of OA4, the Examiner states:

A mere format change by rearranging the position of the Appendices (i.e. placing them prior to the claims recitation section) would be of minor consequence. Here, however, Applicants have not only placed the Appendices before the claims but also edited and extracted sections of both Appendices and placed them in the formal specification.

Reformatting of a specification, to satisfy all formalities, is routine and yet the Examiner would seem to bar us from accomplishing this. The Examiner seems to assert that Appendices A and B can be reformatted to the extent of changing their location to before the claims, but that no further changes can be made. The Examiner has cited no rule to support such an assertion and applicants are aware of no such Patent Office rule.

Applicants introduced, in RT OA2, minimal changes to the specification and figures, consistent with expressing Appendices A and B in formal form. More specifically, RT OA2 accomplishes only the three following changes. First, for each of Appendices A and B, its figures and text are copied to separate sheets. Second, captions to the figures of Appendices A and B are appended, as-is, to the section of the formal specification called "A Brief Description of the Drawings." Third, the text of Appendices A and B is moved to just before the claims. In order to emphasize that none of these three changes add new matter, each change is discussed in further detail below.

Figures 1(a)-1(c), 2(a)-2(b), 3, 4(a)-4(c), 5(a)-5(b), 6(a)-6(d), 7(a)-7(b), 8(a)-8(d), 9(a)-9(b) of Appendix A correspond to, respectively, the following Figures added by RT OA2: 29(a)-29(c), 30(a)-30(b), 31, 32(a)-32(c), 33(a)-33(b), 34(a)-34(d), 35(a)-35(b), 36(a)-36(d), 37(a)-37(b). Each figure of Appendix A is exactly copied to a formal drawing sheet. The caption for each figure of Appendix A is appended, as-is, to the section of the formal specification called "A Brief Description of the Drawings."

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Figures 1, 2(a)-2(b), 3, 4, 5, 6, 7(a)-7(b) and 8 of Appendix B correspond to, respectively, the following Figures added by RT OA2: 38, 39(a)-39(b), 40, 41, 42, 43, 44(a)-44(b) and 45. Each figure of Appendix B is exactly copied to a formal drawing sheet. The caption for each figure of Appendix B is appended, as-is, to the section of the formal specification called "A Brief Description of the Drawings."

The text of Appendix A and the text of Appendix B is inserted, as-is, just before the claims section of the specification.

Despite the fact that the text and figures, of Appendices A and B, were moved "as-is" to the formal drawings and the specification, the Examiner asserts that applicants have added new matter. For example, the Examiner states:

Applicants have not only placed the Appendices before the claims but have also edited and extracted sections of both Appendices and placed them in the formal specification.

OA4, paragraph 7.

Assuming the Examiner agrees that the Appendices are part of the specification as originally filed, the above statement by the Examiner is in direct opposition to Patent Office policy that permits informalities to be corrected. For example, separation of figures from text is addressed by MPEP 608.01, under the heading "ILLUSTRATIONS IN THE SPECIFICATION." This portion of the MPEP states:

Graphical illustrations, diagrammatic views, flow-charts, and diagrams in the descriptive portion of the specification do not come within the purview of 37 CFR 1.58(a), which permits tables, chemical and mathematical formulas in the specification in lieu of formal drawings. The examiner should object to such descriptive illustrations in the specification and request formal drawings in accordance with 37 CFR 1.81 when an application contains graphs in the specification.

Since Appendices A and B are also properly incorporated by reference, as discussed in section 3 "Incorporation By Reference," the above statement by the Examiner is also in direct opposition to MPEP 608.01(p)I.A.2, which states that improper incorporation of essential subject matter can be fixed by amending the specification to include the material incorporated by reference. MPEP 608.01(p)I.A.2 must permit for movement of text and drawings, from material incorporated by reference, to the appropriate locations in a formal specification.

Rather than addressing either of these bases for applicants amendments to the Appendices, the Examiner makes the conclusory statement, in the above quote from OA4, paragraph 7, that the Appendices have been "edited," but provides not one example of such supposed editing.

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Other statements by the Examiner, to support a rejection of Appendix formalization based on new matter, are similar. For example, the Examiner states:

Applicants may not weave text or drawing sections from the Appendices into the subject matter of the formal specification, nor may Applicants edit the non-patent literature.

OA4, paragraph 8. Once again, Patent Office policy permits informalities to be corrected and incorporation by reference permits for movement of text and drawings, from material incorporated by reference, to the appropriate locations in a formal specification. The Examiner makes the conclusory statement that one cannot "weave" text or drawings of the Appendices into the formal specification, but provides not one example of a "weave" nor any explanation of why it would constitute new matter.

A third example statement by the Examiner, in support of a new matter rejection under 35 U.S.C. 132, is as follows:

Applicants' extraction of the Appendices sections and insertion of those same sections into the formal specification is improper and the inserted sections must be deleted from the formal specification. Further, Applicants have edited the contents of the Appendices (i.e. the text of the non-patent literature has been substantially edited).

OA4, paragraph 12. Once again, the Examiner has not stated why "extraction" and "insertion" of sections runs contrary to Patent Office policy, either for purposes of correcting informalities or for purposes of incorporating essential subject matter directly into an application. Further, the Examiner makes the conclusory statement that the Appendices have been "substantially edited" without providing even one example of substantial editing.

By making only conclusory assertions, without reference to specific examples or Patent Office rules, applicants respectfully submit that the Examiner is not following the policy stated in MPEP section 706:

The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity.

Applicants respectfully request a unambiguous statement that Appendices A and B now meet all Patent Office formalities. Applicants respectfully request an unambiguous statement that applicants formalization of Appendices A and B does not introduce new matter under any statute or regulation, including under 35 U.S.C. 251, 35 U.S.C. 132 and 37 CFR 1.173(a).

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3. Incorporation By Reference

The Examiner rejects incorporation by reference, of Appendices A and B, for the following reasons.

In paragraph 6 of OA4 the Examiner states:

Appendices A and B are non-patent literature. ... [A]t the time of the original application filing, both pieces of non-patent literature in Appendix A and B were unpublished documents. Unpublished documents cannot be incorporated by reference.

In paragraph 10 of OA4 the Examiner states:

Applicants attempt to incorporate by reference publications with publication dates that are later (June 12-16, 1995) than the filing date of the original application (May 12, 1995). Literature that was not published or in the public domain at the time of application filing cannot be incorporated by reference.

In paragraph 22 of OA4 the Examiner states:

The MPEP provides policy on the incorporation by reference of non-essential subject matter. "Nonessential subject matter may be incorporated by reference to ... (3) **non-patent publications**. (emphasis added). Most notably, the subject matter of Applicants' Appendices A and B were not publications at the time of the filing of the original application 08/440,554, so incorporation by reference is inapplicable. ... Since a disclosure must be complete as of the time of the filing date, Applicants' attempt to incorporate by reference this non-patent literature is improper.

In the above quotation from paragraph 22, the Examiner is referring to MPEP 608.01(p)I.A ("Review of Applications Which Are To Issue as Patents"). Contrary to the Examiner's characterization of it, the portion of the MPEP relied upon by the Examiner makes no statement that a non-patent publication must be published at the time the referencing application is filed.

With regard to incorporation by reference of essential material, MPEP 608.01(p)I.A.1 ("Complete Disclosure Filed") does specifically state that, prior to allowance, if a referenced application has not been published or issued, the applicant will be required to amend the disclosure of the referencing application to include the material incorporated by reference. Thus, for essential material, the MPEP is specific that publication need not have occurred as of the time the referencing application is filed.

The part of MPEP 608.01(p) most applicable to the current situation is MPEP

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608.01(p)I.A.2 ("Improper Incorporation"). MPEP 608.01(p)I.A.2 states that improper incorporation of essential subject matter, by reference to a foreign application or patent or to a publication, can be fixed by amending the specification to include the material incorporated by reference. MPEP 608.01(p)I.A.2 cites to *In re Hawkins*, 486 F.2d 569 (CCPA 1973). A summary of *In re Hawkins* follows.

In *In re Hawkins*, the Examiner rejected all claims on the grounds that certain British patent applications, needed for essential subject matter, were unavailable to the public as of the time of filing. *In re Hawkins* at 571. The applicant responded to the rejection by deleting the cross references to the British applications and replacing them with essentially all the disclosure contained in the British applications, in an amendment approximately 44 pages long. *Id.* However, the Examiner maintained it was improper to incorporate subject matter which was not available in the United States Patent Office at the time of filing. *In re Hawkins* at 572. The court, however, held that the function of section 112, to ensure complete public disclosure, is only violated if the disclosure is not complete at the time of issuance. *In re Hawkins* at 574. The court stated: "Whether or not the material was secret at any particular time is irrelevant." *In re Hawkins* at 575. With regard to the specific application at issue, the court concluded:

[W]e find that the addition to the disclosure of the textual material originally incorporated by reference cured any defects it might have originally had as filed, and that the application is in compliance with section 112 of the statute.

In re Hawkins at 575.

Since it is proper to incorporate by reference subject matter that is not published at the time of filing, so long as it is published at the time of issuance, incorporation by reference of Appendices A and B is proper for at least the following reasons.

First, Appendices A and B were published, in a conference proceedings, one month after the referencing application was filed and three years before the referencing application issued as a patent.

Second, Appendices A and B were published, concurrent with the issuance of the referencing application, by virtue of their inclusion in the USPTO file history of the referencing application. This is in accordance with USPTO policy, as stated in MPEP 2128 ("A REFERENCE IS A 'PRINTED PUBLICATION' IF IT IS ACCESSIBLE TO THE PUBLIC").

4. Extent of Incorporation By Reference

Applicants have shown in section 3 ("Incorporation By Reference") that Appendix B is properly incorporated by reference and that the text of the formal specification can be augmented in accordance with MPEP 608.01(p)I.A.2. Therefore, the issue addressed in this section is as follows: the extent to which Appendices A and B can be textually incorporated into the formal specification.

The Examiner states: "even if the incorporation of the publications were

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somehow considered proper ... [a]pplicant is only entitled to that portion of the publication that contains subject matter specifically referenced in the application." OA4, paragraph 11. Even assuming the Examiner has stated the correct standard for limiting the material that can be moved through an incorporation by reference, the specification's references to Appendices A and B satisfy this standard.

The specification refers to Appendix B in a section entitled "Scheduling Modes." Specification, page 3, line 24 to page 4, line 9. The specification refers to Appendix B (at page 4, line 4) as a reference where "[s]cheduling modes are discussed further."

Even a casual examination of Appendix B shows that it is entirely about scheduling modes. For example, the first two sentences of Appendix B, that begin the "Overview" section 1.0, are as follows (emphasis in original):

This paper describes a synthesis methodology that uses high-level synthesis (HLS) of behavioral hardware-description language (HDL) descriptions. HLS has the distinguishing characteristic that operations are automatically *scheduled*, i.e. assigned to states, as opposed to lower-level synthesis, in which operations are assigned to states by the user.

The structure of Appendix B is previewed in section 1.1 of the Overview. As can be seen, section 2 provides material relevant to the discussion, of scheduling modes, in following sections 3-7. Each of sections 3, 4 and 5 discusses a particular scheduling mode in detail. Section 6 summarizes experience with actual use of such scheduling modes. Section 7 summarizes the discussion of scheduling modes presented in the paper's preceding six sections.

The specification refers to Appendix A in the paragraph at page 14, lines 11-19. The specification refers to Appendix A (at page 14, line 12) as a reference where "[t]emplates are described." The specification introduces templates (at page 14, line 11) as "[a]n additional technique used for scheduling."

Even a casual examination of Appendix A shows that it is entirely about the use of templates for scheduling. For example, the title of Appendix A states it is about "Scheduling using Behavioral Templates." The first sentence of the abstract states: "This paper presents the idea of 'behavioral templates' in scheduling."

Since applicants have shown that the entirety of Appendices A and B are specifically referenced in the application, the entirety of Appendices A and B is available for putting into formal form.

5. Claim Rejections – 35 USC § 251

Claims 35-40 are rejected by the Examiner as being based upon new matter from Appendix B. OA4, paragraph 17. Specifically, the Examiner states:

Applicants' formal specification as originally filed does

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not include support for the term "clock statement".
Applicants' Appendices A and B may not be referenced in
the specification as being "incorporated by reference".

OA4, paragraph 15.

Since applicants have already shown above that Appendix B is now part of the formal specification (by being part of the specification as-filed and by incorporation by reference), applicants respectfully traverse this rejection.

6. Claim Rejections – 35 USC § 112 ¶ 1

Claims 35-40 are rejected by the Examiner as not enabled due to their being based upon new matter from Appendix B. OA4, paragraph 17.

Since applicants have already shown above that Appendix B is now part of the formal specification, applicants respectfully traverse this rejection.

7. Discussion with OPLA

In RT OA3, page 12 of 14, applicants buttress their argument, that the Appendices are part of the original application as-filed, by stating the following regarding applicants discussions with the USPTO Office of Patent and Legal Administration (OPLA):

Applicants have discussed this issue with the USPTO
Office of Patent Legal Administration, and it is in agreement
with the applicants.

In response, the Examiner states:

Examiner encourage Applicants to review 37 C.F.R.
1.2 which should remind Applicants that off the record and
hearsay discussions do not carry any weight or merit during
patent prosecution before the USPTO.

OA4, paragraph 23.

At the suggestion of the Examiner, applicants have reviewed 37 CFR 1.2. The rule merely requires that all business with the USPTO be conducted in writing and contains no bar against presenting written hearsay-type evidence to an examiner in a response to an Office Action.

Applicants presented hearsay-type evidence, of the results of its discussions with OPLA, in an effort to reach a resolution, on the issue of new matter raised by the Examiner, as soon as possible.

Certainly, OPLA is an authoritative body within the USPTO. Furthermore, a hearsay-type objection, to applicants presentation of an opinion of OPLA, is not appropriate where the Examiner is able to contact OPLA independently to confirm OPLA's agreement with applicants.

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(viii) Claims appendix

1. A method performed by a data processing system having a memory, comprising the steps of:

parsing a text description of a circuit, said text description stored in the memory, said text description including a loop with a delayed signal assignment having a delay value;

translating said text description into a digital circuit representation in said memory, said digital circuit representation including a pipeline; and

setting a latency of said pipeline equal to said delay value.
2. The method of claim 1, wherein said loop further includes N wait statements, where N is greater than zero, said method further comprising the step of setting an initiation interval of said pipeline equal to N.
18. A system for building, in a memory, a digital circuit representation which implements the behavior of a text description in said memory, said system having a processor coupled to a memory unit wherein said processor is programmed to perform logic processing, said system comprising:

parsing logic for parsing said text description into a parsed text description, said text description including a loop with a delayed signal assignment having a delay value;

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translating logic for translating said parsed text description into said digital circuit representation, said digital circuit including a pipeline; and

latency setting logic for setting a latency value of said pipeline to be said delay value of said delayed signal assignment.

21. A computer program product comprising:

a computer usable medium having computer readable code embodied therein for building a digital circuit representation from a text description of a digital circuit, the computer program product comprising:

computer readable program code devices configured to cause a computer to effect parsing said text description, said text description including a loop with a delayed signal assignment having a delay value;

computer readable program code devices configured to cause a computer to effect translating said text description into said digital circuit representation including a pipeline; and

computer readable program code devices configured to cause a computer to effect setting a latency of said pipeline equal to said delay value.

35. The method of claim 1[2], wherein said loop further includes N clock statements, where N is greater than zero, said method further comprising the step of setting an initiation interval of said pipeline equal to N.

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36. A system as described in claim 18, wherein said loop further includes a number, n, of clock statements, said system further comprising initiation interval setting logic for setting an initiation interval of said pipeline to be equal to n.

37. The computer program product of claim 21 wherein said loop further includes N clock statements, where N is greater than zero, said computer program product further comprising computer readable program code devices configured to cause a computer to effect setting an initiation interval of said pipeline equal to N.

38. A method performed by a data processing system having a memory, comprising the steps of:

parsing a text description of a circuit, said text description stored in the memory, said text description including a loop with N clock statements, where N is greater than zero;

translating said text description into a digital circuit representation in said memory, said digital circuit representation including a pipeline; and

setting an initiation interval of said pipeline equal to N.

39. A system for building, in a memory, a digital circuit representation which

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implements the behavior of a text description in said memory, said system having a processor coupled to a memory unit wherein said processor is programmed to perform logic processing, said system comprising:

parsing logic for parsing said text description into a parsed text description, said text description including a loop with N clock statements, where N is greater than zero;

translating logic for translating said parsed text description into said digital circuit representation, said digital circuit including a pipeline; and

initiation interval setting logic for setting an initiation interval of said pipeline equal to N.

40. A computer program product comprising a computer usable medium having computer readable code embodied therein for building a digital circuit representation from a text description of a digital circuit, the computer program product comprising:

computer readable program code devices configured to cause a computer to effect parsing said text description, said text description including a loop with N clock statements, where N is greater than zero;

computer readable program code devices configured to cause a computer to effect translating said text description into said digital circuit representation including a pipeline; and

computer readable program code devices configured to cause a computer to

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effect setting an initiation interval of said pipeline equal to N.

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(ix) Evidence appendix

None.

(x) Related proceedings appendix

None.

Respectfully submitted,

/ Jonathan T. Kaplan /

Jonathan T. Kaplan (Reg. No. 38,935)

Date: Jul. 20, 2006
JONATHAN T. KAPLAN
ATTORNEY AT LAW
10800 SE 17TH CIRCLE, SUITE E66
VANCOUVER, WA 98664-6297
TEL. 917-674-6017